IN THE DRAWINGS

Please add FIGs. 14-18 filed concurrently with this preliminary amendment.

IN THE SPECIFICATION

Please add the following sentence as the first paragraph following the title.

The present application is based on prior U.S. application No. 09/849,720, filed on May 4, 2001, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed.

On page 2, line 33, modify paragraph **[0007]** as follows. This is a marked-up version of paragraph **[0007]**.

[0007] FIG. 1 is an application diagram illustrating a TVS device;

FIG. 2 is a diagram illustrating a Metal Oxide Semiconductor (MOS) device used as a low voltage, TVS device;

FIG. 3 is a schematic diagram illustrating the equivalent circuit of the voltage suppression device of FIG. 2;

FIG. 4 is a threshold curve useful in explaining the operation of the TVS device of FIG. 2;

FIG. 5 is a diagram illustrating a MOS device used as a symmetrical, clipping TVS device;

FIG. 6 is a schematic diagram illustrating the equivalent circuit of the symmetrical, clipping TVS device of FIG. 5;

FIG. 7 is a threshold curve useful in explaining the operation of the symmetrical TVS device of FIG. 5;

FIG. 8 illustrates a MOS device with an integral gate-drain connection used as a TVS device;

FIG. 9 illustrates an alternate MOS device with an integral gate-drain connection used as a TVS device;

FIG. 10 illustrates a trench MOS device used as a TVS device;

FIG. 11 illustrates a modified trench MOS device with topside drain contact;

FIG. 12 illustrates an alternate trench device used as a TVS device; and

FIG. 13 illustrates a lateral MOS device used as a TVS device;

FIG. 14 is a schematic diagram of an integrated circuit including an insulated gate bipolar transistor (IGBT)_-based TVS device;

FIG. 15 is a cross-sectional view of the IGBT-based TVS device;

FIG. 16 is a cross-sectional view of the IGBT-based TVS device in an alternate embodiment;

FIG. 17 is a cross-sectional view of an IGBT-based TVS device with an alternate gate biasing arrangement; and

FIG. 18 is a cross-sectional view of the TVS device in a planar embodiment.

Following is paragraph **[0007]** in clean form.

[0007] FIG. 1 is an application diagram illustrating a TVS device;

FIG. 2 is a diagram illustrating a Metal Oxide Semiconductor (MOS) device used as a low voltage, TVS device;

FIG. 3 is a schematic diagram illustrating the equivalent circuit of the voltage suppression device of FIG. 2;

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FIG. 16 is a cross-sectional view of the IGBT-based TVS device in an alternate embodiment;

FIG. 17 is a cross-sectional view of an IGBT-based TVS device with an alternate gate biasing arrangement; and

FIG. 18 is a cross-sectional view of the TVS device in a planar embodiment.

Please insert the following text on page 11, line 1, i.e., after paragraph **[0023]**.

[0024] FIG. 14 shows a schematic diagram of an integrated circuit 200 including an IGBT-based TVS device 201 housed in a semiconductor package 210 having a lead 208 coupled to an external bus 215 and a lead 209 operating at ground potential. Bus 215 carries an information signal V_{DATA} that operates between zero and two volts, and is susceptible to a high energy, high voltage transient signal V_{TRANS} that is induced by electrostatic discharge or a line disturbance and effectively superposed on information signal V_{DATA}.

[0025] TVS device 201 includes an IGBT 202 and back-to-back diodes 203-204. IGBT 202 is coupled across leads 208-209 of semiconductor package 210 to dissipate the energy induced by V_{TRANS} by turning on when V_{TRANS} is greater than a predefined level. Energy is dissipated by shunting an associated surge current I_{TRANS} when V_{TRANS} reaches the predefined level typically set by adjusting the gate-emitter conduction threshold of IGBT 202 during fabrication by

varying the dopant level that is implanted in the channel region to adjust the conduction threshold of the device.

[0026] Integrated circuit 200 may include an input transistor 212 whose source and gate electrodes are coupled to leads 208-209, respectively, for coupling V_{DATA} to other circuitry of integrated circuit 200. Its gate electrode is coupled to lead 208 and formed to operate at an amplitude less than its gate rupture potential which, in one embodiment, is about twenty volts. TVS device 201 protects the gate oxide of transistor 212 from being ruptured by an excessive electric field by clamping V_{TRANS} to limit its voltage magnitude. Alternatively, TVS device 201 could be formed as a two-lead stand alone integrated circuit that suppresses transient signals on external data and/or power supply lines to protect external circuitry.

[0027] IGBT 202 may be either a vertical or planar device that is configured to present leads 208-209 with a low capacitance. Doping levels are selected so that IGBT 202 has a gate-emitter conduction threshold of about 2.3 volts and a low subthreshold collector-emitter leakage current. A gate terminal 213 is connected with an interconnect line 241 to a collector terminal and to lead 208, while an interconnect line 240 operates as an emitter terminal connected to lead 209, which operates at ground potential. The gate connection results in IGBT 202 turning on when the voltage on lead 208 is greater than about 2.3 volts. Consequently, when lead 208 operates between zero and two volts, i.e., within the V_{DATA} range, TVS device 201 operates as a substantially open circuit, while turning on to shunt current when its gate voltage exceeds about 2.3 volts to effectively clamp lead 208 to a voltage level less than about five volts.

[0028] Diodes 203-204 are formed on the same die as IGBT 202 and configured to protect the IGBT 202 gate from destructively breaking down when V_{TRANS} undergoes a negative transition. When V_{TRANS} is negative, diode 203 is forward

biased while diode 204 is reverse biased. Diodes 203-204 are doped to breakdown at a voltage in a range between six and seven volts. Depending on the gate oxide breakdown or rupture voltage in a particular application, virtually any number of series-connected back-to-back diodes can be formed between the emitter and gate terminals of IGBT 202 to set the protection voltage to a value less than the rupture voltage. For example, in an embodiment where the gate oxide rupture voltage is twenty volts, two pairs of serially connected back-to-back diodes can be used to maintain the gate voltage less than twelve volts.

[0029] To see the operation of TVS device 201, assume that input transistor 212 has a destructive gate to source breakdown or gate oxide rupture of five volts and that IGBT 202 is doped to have a conduction threshold V_{TH}=2.3 volts.

[0030] Since IGBT 202 has a low capacitance as well as a higher conduction threshold than the amplitude of V_{DATA}, under normal conditions, TVS device 201 effectively operates as an open circuit with respect to leads 208-209. Now assume an electrostatic discharge or other system event induces a five ampere transient signal V_{TRANS} on bus 215 at a voltage level greater than V_{TH}=2.3 volts. TVS device 201 turns on to shunt a transient current I_{TRANS} generated by V_{TRANS}, thereby dissipating the transient energy and clamping the voltage at the gate of transistor 212 to a value less than five volts. I_{TRANS} causes internal regions of IGBT 202 to be conductivity modulated, which results in a low on-state resistance and low voltage drop. For example, in an embodiment in which IGBT 202 has an effective active area of about 0.7 millimeters^2, TVS device 201 can clamp lead 208 to a voltage level of less than about five volts while shunting five amperes of peak I_{TRANS} current. Consequently, the gate of input transistor 212 is maintained below its destructive rupture value, which avoids permanent damage to transistor 212 and increases the reliability of integrated circuit 200.

[0031] FIG. 15 is a cross-sectional view of integrated circuit 200 including IGBT 202 and diodes 203-204 of TVS device 201 as formed on a semiconductor substrate 220. In one embodiment, IGBT 202 is implemented as an n-channel device.

[0032] A sublayer 216 is formed at a bottom surface 236 of substrate 220 and heavily doped to have a p-type conductivity to operate as low-resistance collector terminal of IGBT 202. The heavy doping levels also ensure that a uniform, high quality ohmic contact can be made to bottom surface 236. In one embodiment, sublayer 216 is made of monocrystalline silicon.

[0033] An epitaxial layer 217 is formed over sublayer 216 to operate as a drift region of IGBT 202. Epitaxial layer 217 is lightly doped to have an n-type conductivity so that its metallurgical junction with sublayer 216 has a low capacitance in order to present a minimal reactive load so that TVS device 201 operates as substantially an open circuit when IGBT 202 is turned off. In one embodiment, epitaxial layer 217 is formed to a thickness of about twelve micrometers and a doping concentration of about 10^{14} atoms/centimeter^3.

[0034] A body region 228 is formed by diffusing p-type impurities into epitaxial layer 217 through a top surface 236 of semiconductor substrate 220. In one embodiment, body region 228 has a depth of about two micrometers. In the plane of FIG. 15, integrated circuit 200 is shown as having two body regions 228. However, these regions are electrically coupled together out of the view plane so as to effectively comprise a single body region 228.

[0035] A body contact region 224 is formed in body region 228 to provide an ohmic contact at top surface 238. Accordingly, body contact region 224 is heavily doped to have a p-type conductivity and is formed to a depth of, for example, 0.6 micrometers.

[0036] An emitter region 222 is formed at top surface 238 within body region 228. In one embodiment, emitter region 222 is heavily doped with an n-type conductivity and a depth of about 0.15 micrometers.

[0037] A dielectric material is formed over surface 238 to provide a gate dielectric 214 of IGBT 202. In one embodiment, gate dielectric 214 comprises thermally grown silicon dioxide formed to a thickness of about two hundred fifty angstroms.

[0038] A conductive material is deposited over surface 238 and patterned to form a gate terminal 213 of IGBT 202 over gate dielectric region 214. In one embodiment, gate terminal 213 is formed with doped polycrystalline silicon to function with gate dielectric 214 as a gate structure of IGBT 202.

[0039] The conductive material is further patterned to form cathode regions 205 and 207 and a common anode region 206 over a dielectric region 242. Cathode regions 205 and 207 are doped to have an n-type conductivity and common anode region 206 is doped to have a p-type conductivity. Back to back diodes 203 and 204 result from the metallurgical junctions of common anode region 206 with cathode region 205 and cathode region 207, respectively, as shown. Diodes 203-204 are doped to break down in a range between about six and about seven volts to prevent damage to gate dielectric 214 during a negative-going V_{TRANS} voltage spike. Two additional series-coupled back-to-back diodes are typically added to increase the protection voltage to a range between about twelve volts and about fourteen volts.

[0040] A metal layer is deposited and patterned to form interconnect line 240 that operates as an emitter terminal. Interconnect line 240 is connected to emitter region 222, to body contact region 224 and to anode region 207 of diode 203. The metal layer is further patterned to produce

interconnect line 241 to connect gate terminal 213 to anode 205 of diode 204 as shown.

[0041] Semiconductor substrate 220 is mounted on a die flag 232 of semiconductor package 210 with a die attach material that has a low electrical and thermal resistance. In one embodiment, die flag 232 is formed with a low resistance metal such as copper. In one embodiment, die flag 232 operates as lead 208 to provide a low external connection to integrated circuit 200. External connections to lead 209 are made with a standard wire bond or clip lead arrangement.

[0042] A bonding wire 234 connects anode 205 of diode 204 to die flag 232 so that gate terminal 213 and collector region or terminal 216 operate at substantially the same potential.

[0043] In operation, a positive excursion of transient signal V_{TRANS} is coupled through die flag 232, bonding wire 234 and interconnect line 241 to gate terminal 213. If the amplitude of V_{TRANS} is greater than the conduction threshold of IGBT 202, body region 228 inverts under gate terminal 213 to form a channel 230 that allows surge current I_{TRANS} to flow through IGBT 202 along a current path 249 as shown. IGBT 202 is referred to as a vertical transistor because I_{TRANS} flows vertically through the device between top surface 238 and bottom surface 236.

[0044] Surge current I_{TRANS} causes a junction 251 between sublayer 216 and epitaxial layer 217 to forward bias, injecting minority carriers into sublayer 216 and epitaxial layer 217. The minority carriers conductivity modulate epitaxial layer 217, so that its resistivity is reduced, which reduces the on-state resistance of IGBT 202. Because epitaxial layer 217 is lightly doped to provide a low junction 251 capacitance, the conductivity modulation of can result in an effective resistivity reduction of several orders of magnitude at high I_{TRANS} current levels. For

example, at a peak I_{TRANS} current of one hundred amperes, the effective resistance of epitaxial layer 217 can be reduced by as much as a factor of three. As a result, IGBT 202 has a high gain, so large I_{TRANS} current levels are accommodated with only a small increase in potential on lead 208. In effect, I_{TRANS} is shunted to ground potential to dissipate the energy stored in V_{TRANS}, thereby clamping the voltage on lead 208 to a level that avoids damaging other components of integrated circuit 200. For negative V_{TRANS} excursions, back-to-back diodes 203-204 break down to clamp the potential on gate terminal 213 to prevent gate rupture or other damage to gate dielectric region 214.

[0045] FIG. 16 is a cross-sectional view of TVS device 201 in an alternate embodiment. The structure and operation of this embodiment are similar to what is described above, except that a collection region 250 is formed between portions of body region 228 as shown. Collection region 250 typically is formed using the same processing steps as body region 228, and consequently has a p-type conductivity and similar junction depth and doping concentration. A p-type collection contact region 252 is formed within collection region 250 at top surface 238. Region 252 is heavily doped and typically formed during the same processing steps used to form region 224 to ensure a high quality ohmic contact to collection region 250.

[0046] Sublayer 216, epitaxial layer 217 and collection region 250 operate as an emitter, base and collector, respectively, of a merged PNP bipolar transistor 253 that provides a current path 254 between leads 208-209 that is parallel to current path 249 of IGBT 202. When IGBT 202 turns on, surge current I_{TRANS} forward biases junction 251, causing minority carrier holes to be injected into epitaxial layer 217. The holes are collected by collection region 250 as a V_{TRANS} component current I_{PNP} that is summed with I_{TRANS} and routed through leads 208-209 to increase the transconductance gain and overall current capability of TVS

device 201, thereby improving both performance and reliability.

[0047] FIG. 17 is a cross-sectional view of TVS device 201 in another alternate embodiment. The structure and operation are similar to the embodiments described above, except as follows.

[0048] A drift contact region 260 is formed in epitaxial layer 217 to provide an ohmic contact at surface 238. In one embodiment, drift contact region 260 is heavily doped to have an n-type conductivity using the same processing steps as region 222 to operate at substantially the same potential as epitaxial region 217.

[0049] Gate terminal 213 is connected through interconnect line 241 to drift contact region 260 to bias gate terminal 213 at the same potential as epitaxial region 217. Hence, gate terminal 213 is biased through forward-biased junction 251, rather than by a direct connection to lead 208. Consequently, in response to transient voltage V_{TRANS}, the voltage level on lead 208 is about 0.6 volts higher than what it would be if gate terminal 213 were connected to lead 208 through a bonding wire. Since no bonding wire is needed to bias gate terminal 213, the FIG. 17 embodiment typically has a lower inductance and therefore a faster response and lower cost.

[0050] FIG. 18 is a cross-sectional view of TVS device 201 in an embodiment as a planar or lateral device. The operation and structure are similar to those described above except as follows.

[0051] Sublayer 216 has an n-type conductivity and typically may be heavily doped to provide a ground plane, especially if other circuitry besides TVS device 201 is integrated on substrate 220. Hence, sublayer 216 and epitaxial layer 217 have the same conductivity type.

[0052] A p-type collector region 270 is formed in epitaxial layer 217 using the same processing steps as those

used to form body region 228. A collector contact region 272 is formed at top surface 238 within collector region 270. Collector contact region is heavily doped to provide a good ohmic contact for operating as a collector terminal of IGBT 202.

[0053] A junction 271 is formed between epitaxial layer 217 and collector region 270, both of which are relatively lightly doped and therefore provide a low capacitance load to devices protected by TVS device 201. Gate terminal 213 is connected directly to lead 208 and collector contact region 272 with interconnect line 241 as shown to operate at the same potential as the collector terminal.

[0054] When IGBT 202 turns on in response to transient signal V_{TRANS}, surge current I_{TRANS} flows from channel 230 laterally, i.e., in a direction parallel to top surface 238, along a current path 279 through collector region 270, collector contact region 272 and interconnect line 241 to lead 208 as shown. Junction 271 forward biases to inject minority carriers into both epitaxial layer 217 and collector region 270, thereby conductivity modulating both regions and producing a low resistance path that enhances the current capability of TVS device 201.

[0055] External connections are made through leads 208-209, both of which are formed at top surface 238 and connected with standard wire bond or clip techniques.

Please replace or renumber former paragraph **[0024]** as paragraph **[0056]**. A marked-up version is shown below.

~~**[0024]**~~**[0056]** In summary, several methods of providing a TVS device using MOS and IGBT structures are presented. The TVS devices exhibit superior leakage current performance, while allowing for clamping voltages in the sub-5 volt range. Clamping voltages between 0.5 volts and 5 volts are readily available through implantation control and high gain allows relatively constant clamping voltage characteristics.

A clean version of former paragraph **[0024]** is shown below.

[0056] In summary, several methods of providing a TVS device using MOS and IGBT structures are presented. The TVS devices exhibit superior leakage current performance, while allowing for clamping voltages in the sub-5 volt range. Clamping voltages between 0.5 volts and 5 volts are readily available through implantation control and high gain allows relatively constant clamping voltage characteristics.